IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC, **Plaintiff,** **v.** **HTC CORPORATION and HTC AMERICA, INC.,**	**Case No. 2:14-cv-00690-JRG-RSP (Lead)**
LG ELECTRONICS, INC., et al., **Defendants.**	**Case No. 2:14-cv-00691-JRG-RSP (Consolidated)**

DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

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Exhibit 18	Excerpts from Franklin, M., "Computer Architecture and Organization: From Software to Hardware," University of Maryland, 2007, PRIOR-ART_0024645
Exhibit 19	Excerpts from Stallings, W., "Computer Organization and Architecture," Prentice Hall, 1996, 4th ed., PRIOR-ART_0025433
Exhibit 20	Excerpts from Stone, H., "Microcomputer Interfacing," Addison-Wesley Publishing Company, 1982, PRIOR-ART_0000509
Exhibit 21	U.S. Patent No. 5,093,890 to Bregman et al.

Note: Defendants have not included the Asserted Patents as exhibits. They are attached to PUMA's brief as Exhibits A-I. Furthermore, Exhibits 17-20 are cited only in the Declaration of Dr. Harold Stone, attached as Exhibit 2.

TABLE OF ABBREVIATIONS

PUMA	Plaintiff Parthenon Unified Memory Architecture, LLC
PUMA Br.	PUMA's Opening Claim Construction Brief
'789 patent	U.S. Patent No. 5,812,789
'464 patent	U.S. Patent No. 5,960,464
'459 patent	U.S. Patent No. 6,058,459
'194 patent	U.S. Patent No. 6,427,194
'368 patent	U.S. Patent No. 7,321,368
'045 patent	U.S. Patent No. 7,542,045
'753 patent	U.S. Patent No. 7,777,753
'315 patent	U.S. Patent No. 8,054,315
'164 patent	U.S. Patent No. 8,681,164
Related Patents	Collectively the '789 patent, the '459 patent, the '194 patent, the '368 patent, the '045 patent, the '753 patent, the '315 patent, and the '164 patent, i.e., all except the '464 patent.
Asserted Patents	Collectively the '464 patent and the Related Patents

I. INTRODUCTION

PUMA proposes broad constructions unsupported by the intrinsic record in an attempt to stretch its infringement read far beyond the bounds of what the inventors claimed. Despite over seventeen years of prosecution for the patents at issue, PUMA fails to cite *even a single page* from the file histories to support its arguments. In contrast, Defendants' constructions are the result of thorough consideration of the claim language and its context, along with both intrinsic and extrinsic evidence, and should, therefore, be adopted.

II. RELEVANT LEGAL STANDARDS

The Court is well versed in the general principles of claim construction. The process of construing a claim term begins with the words of the claims themselves. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc). However, the claims "must be read in view of the specification, of which they are a part." *Phillips*, 415 F.3d at 1315 (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996)). "It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, i.e., the patent itself, including the claims, the specification and, if in evidence, the prosecution history. Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Liquid Dynamics Corp. v. Vaughan Co.*, 355 F.3d 1361, 1367 (Fed. Cir. 2004) (quoting *Vitronics Corp.*, 90 F.3d at 1582).

III. AGREED CONSTRUCTIONS

The parties agree that "simultaneously accesses the bus" should be construed as "accesses the bus at the same time." Furthermore, Defendants withdraw their construction for "without (also) requiring a second bus" and "video stream input device circuit." The parties will rely on plain and ordinary meaning for those terms.

IV. TERMS FOR CONSTRUCTION

A. "bus"

PUMA proposes a construction of "shared bus" that was stipulated in a 2004 case involving only the '789 patent—not the other Related Patents. That construction falls short for two reasons: (1) it fails to distinguish a single bus from multiple buses, which is critical for claims that exclude a second bus,[1] and (2) it does not take into account a statement made during prosecution of the '368 patent requiring a bus to be more than a local, point-to-point connection between two devices. Defendants' proposed construction addresses both shortfalls. Defendants propose the term "bus" be construed as "a signal line or set of parallel signal lines to which a number of devices are attached and over which information may be broadcast among them."

To address the shortfalls of the 2004 construction, Defendants' proposed construction differentiates single and multiple buses, and accounts for the prosecution history statement by (1) changing "transferred" to "broadcast" and adding "parallel" to expressly define the characteristics of a bus, and (2) adding "among them" to reflect the prosecution history statement of connections between just two devices. Defendants' construction also substitutes "attached" for "coupled" to sharpen the construction. Although PUMA objects to "broadcast" and "parallel" as not *literally* appearing within the intrinsic evidence, as described more fully below, these terms impart *concepts* that are pervasive throughout the claims, specification, and file history, and are consistent with the extrinsic evidence.

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[1] *See* '459 patent, claims 1 ("without also requiring a second bus"), 11 ("without requiring a second bus"); *see also* '194 patent, claims 1, 11, 16-18. Neither the '459 patent nor the '194 patent at issue in this case was at issue in the 2004 case.

1. "Broadcast" Reflects a Fundamental Operation of a Bus

"Broadcast" reflects a fundamental property of a "signal line" that distinguishes one bus from multiple buses. A signal line carries only one signal at a time. Ex. 2, Stone Decl. at ¶¶ 33-34. The reason for this is that electronic systems like those disclosed in the Related Patents process data in a binary format (i.e., data in '1's and '0's). *Id.* at ¶ 29. A device seeking to communicate 1 or 0 to another device connected via a signal line drives the signal line with a high or low voltage, respectively. Because the signal line is electrically conductive, the voltage applied appears *everywhere* on the signal line. *Id.* at ¶ 32. As a result, a signal line cannot be used to convey two different signals (e.g., 1 *and* 0) from two different sources at the same time, or else the result is a problematic "contention." Ex. 2 at ¶¶ 33-34. "At best, this [contention] situation will cause garbled data and, at worst, hardware damage." Ex. 1, Anderson at PRIOR-ART_0004775 (incorporated by reference in '789 patent at 12:6-11).

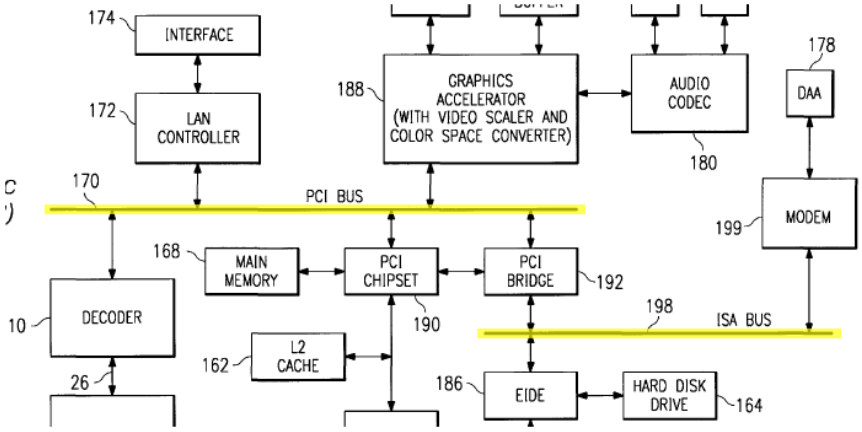
The Related Patents explicitly recognize that only a single device may drive a bus at a time. '789 patent at 3:5-8. To prevent contention, systems include an arbiter that receives requests from the devices to drive the bus and, one at a time, grants the requests. Ex. 2 at ¶ 35. For example, claim 20 of the '368 patent requires "an arbiter coupled to the decoder and to the central processing unit for controlling access to the bus." *See also* '045 patent, cl. 4 and 12. And the specification similarly recognizes the contention issue:

> Each request [for bus access] is typically processed according to a priority scheme. The priority scheme is typically based on the priority given to the device and the order in which the requests are received [by the arbiter].

'789 patent at 3:5-8.

Figure 1c of the '789 patent, excerpted below, shows a block diagram with two buses, PCI bus 170 and ISA bus 198. A signal broadcast on a signal line forming PCI bus 170 would be present everywhere on the signal line and thus available to any device (10, 172, 188, 190, and

192) attached to the PCI bus 170. Similarly, a signal broadcast on a signal line forming ISA bus 198 would be present everywhere on the signal line and thus available to any device (182, 192, 199) attached to ISA bus 198.



To summarize, to "broadcast" information on a signal line of a bus means that the entire signal line carries the same information to the extent of the bus, regardless of the number of devices receiving the information.[2] In contrast, if the signal line is broken into separate parts by an intervening component, switch, etc., so that a device broadcasts to only part of the signal line or so that different devices may transmit information separately on different parts of the signal line, then more than one bus is present.

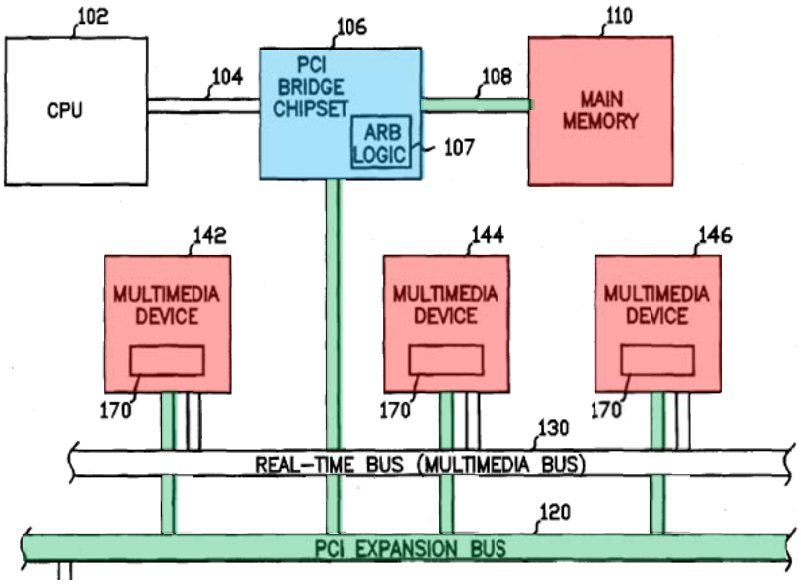
2. "Parallel" Is Required Due to the Specification and File History

If a bus has multiple signal lines, then those lines must be parallel. PUMA's proposed construction, "a set of signal lines . . . over which information may be transferred," is overly broad because it potentially covers configurations that include multiple, separate buses. For

[2] In Defendants' proposed construction, "a signal line or set of parallel signal lines . . . over which information may be broadcast," the term "broadcast" relates to the extent to which information travels on the signal line(s), not the particular number of destinations. Thus, PUMA's reliance on *Tivo, Inc. v. AT&T Inc.*, 2011 WL 6961021 (E.D. Tex. 2011) is inapposite. *See* PUMA Br. at 9.

example, PUMA's proposal suggests that two sequential buses, like PCI bus 170 and ISA bus 198 shown in Figure 1c of the '789 patent above, constitute a single "bus" because "information" may be "transferred" between PCI bus 170 and ISA bus 198 through PCI bridge 192. But, that read contradicts the specifications, the prosecution histories, and the understanding of one of ordinary skill in the art. The '789 patent describes Figure 1c as having *two buses* 170 and 198, not a single bus 170/198 connected through a PCI bridge 192. *See* '789 patent at 3:2-3; *see also* Figure 4 and 9:33-34. Figure 7 in the '459 patent family shows three separate buses 170, 198, and 185. '459 patent at 12:26-27, 40-41.

During the '459 patent's prosecution, Applicants added the limitation *excluding* a second bus to overcome a rejection based on U.S. Patent No. 5,682,484 ("Lambrecht"). Ex. 3, Ex. 4 at PUMA0000686. In response, Applicants argued Lambrecht "is directed to a computer which includes multimedia devices that access a main memory through a PCI bridge chipset." Ex. 5 at PUMA0000763. Lambrecht Figure 1, excerpted and color-coded below, shows that multimedia devices 142, 144, 146 (red) can access main memory 110 (red) via two buses, PCI expansion bus 120 (green) and memory bus 108 (green), that are separated but connected by PCI bridge chipset 106 (blue).



To distinguish Lambrecht, Applicants amended the claims to include a limitation that the decoder has "direct access" to the memory. Ex. 5 at PUMA0000756-57. Applicants argued that Lambrecht "uses a PCI bridge chipset for access between other first devices or decoders and a main memory" and that therefore the "access provided by the PCI bridge chipset is not direct." *Id.* at PUMA0000764. The Examiner then rejected the amended claims as indefinite, stating that it was not "sufficiently clear what was meant by 'direct access.'" Ex. 6 at PUMA0000778. In response, Applicants submitted claims requiring the "first device" and "decoder" be able to access the memory "without requiring a second bus" or "without also requiring a second bus." Ex. 7 at PUMA0000791. The claims were then allowed. Ex. 8 at PUMA0000798.

The prosecution of the '459 patent demonstrates that a "bus," as used in the Related Patents, *cannot* include a set of signal lines that are sequential or in series with other signal lines. The series connection of Lambrecht's memory bus 108, PCI bridge 106, and PCI expansion bus 120 is not a "bus," but rather two sequential buses. The memory bus 108 in Lambrecht is a "bus" that may include a signal line or a set of *parallel* signal lines that are routed to a common set of devices—the PCI bridge chipset 106 and the main memory 110. Similarly, the PCI expansion bus 120 is a "bus" that may include a signal line or a set of *parallel* signal lines that are routed to a common set of devices—multimedia devices 142, 144, 146 and PCI bridge chipset 106. A "set of signal lines" including signal lines in memory bus 108 and signal lines in PCI expansion bus 120 is two buses, not a single bus. Were the series connection of a memory 108, PCI bridge 106, and PCI expansion bus 120 a single bus, the Applicant's amendment to exclude a second bus would have been insufficient to overcome Lambrecht.

3. "Among Them" Accounts for Statements Made During Prosecution

"Among them"—requiring more than two devices—is necessary to account for statements the Applicants made during prosecution of the '368 patent—i.e., interconnections

between only two devices are *not* a bus. Prosecution history is an important source of intrinsic evidence in interpreting claims because it is a contemporaneous exchange between the applicant and the examiner. The public has the right to rely on an applicant's remarks made in seeking allowance of claims. *Desper Prods. Inc. v. QSound Labs. Inc.*, 157 F.3d 1325, 1337 (Fed. Cir. 1998). For example, where an applicant argues that a claim possesses a feature that the prior art does not to overcome prior art, the argument may serve to narrow the scope of otherwise broad claim language. *Seachange Int'l Inc. v. C-COR Inc.*, 413 F.3d 1361, 1372-73 (Fed. Cir. 2005).

The Examiner rejected the then-pending claims of the '368 patent based on U.S. Patent No. 5,576,765 ("Cheney"). Ex. 9, Ex. 10 at PUMA0001210. According to the Applicants, the Examiner was of the "view that there was a bus connected between memory 601 and decoder 201" in Cheney Figure 4, reproduced below, indicating the memory and decoder in red and the connection in blue. Ex. 11 at PUMA0001236.

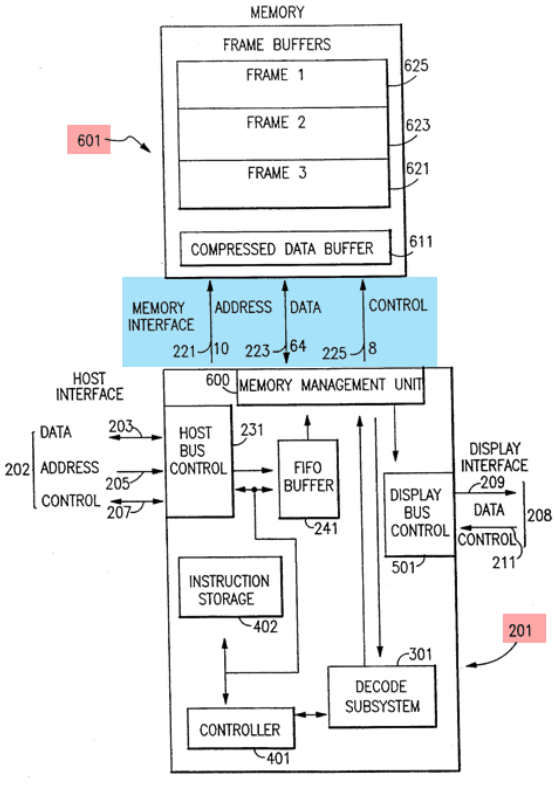


FIG.4

In disputing that the memory-to-decoder connection was a "bus," Applicants argued:

> The connection between memory 601 and decoder 201 is a local connection and connects only the two devices together. *It is not a bus* as was well recognized by Cheney and as is recognized by those with skill in the art.

Id. at PUMA0001236 (emphasis added). Despite the Applicants' characterization, Cheney describes the memory-to-decoder connections as buses. *See* Cheney, Ex. 9 at 7:35-37 ("The interface between the memory management unit 600 [that is part of the decoder 201] and the memory 601 includes an address bus, 221, a bidirectional data bus, 223, and a control bus 225.") Cheney does not describe that connection as a "local connection" anywhere in its specification. Thus, the Applicant's clear and unmistakable statement that the connection between the memory 601 and the decoder 201 is "not a bus" requires the Applicant's "bus" to connect *more than two devices* together. Defendants' use of "among them" in the construction requires *more than two devices* attached to the signal line or set of parallel signals lines.

4. Dr. Stone's Use of "Bus" In His Prior Patent is Consistent with Defendants' Proposal

PUMA cites U.S. Patent No. 5,093,890 as "evidence" that Defendants' proposed construction prohibiting series connections is contradicted by a patent to Defendants' expert, Dr. Stone. PUMA Br. at 9-10. A less selective quotation of the cited patent reveals otherwise:

> In its most basic form, the bus is traditionally a series of electrical lines interconnecting the modules in the computer. Those modules connect to the bus by means of tap lines. In this implementation, the primary bus lines *will not be broken, or rooted through any of the computer modules*.

Ex. 21 at 1:19-24 (emphasis added). That the bus lines "will not be broken" means that the entire line has the same signal, i.e., the signal is *broadcast*. Similarly, the bus lines are not "rooted [sic] through any of the computer modules." Like Lambrecht's PCI bridge chipset 106, signal lines "routed through a module" result in a sequence or series of buses, consistent with Defendants' contention that signal lines comprising a bus must be *parallel*. The description of a "bus" in the '890 patent is consistent with Defendants' proposed construction. Ex. 2 at ¶ 37.

B. "fast bus"

Both parties' proposed constructions for "fast bus" include "real time." Defendants' position is that "real time" is indefinite. *See infra* § IV.C. To the extent the Court finds "real time" to be indefinite, "fast bus" would also be indefinite. Alternatively, if the Court finds "real time" not to be indefinite, Defendants' propose that "fast bus" means a "bus having a bandwidth greater than the bandwidth required for the decoder to operate in real time." Defendants' proposed construction is taken directly from the specification: "The decoder/encoder 80 is coupled to the memory 50 through devices, typically a bus 70[3], that *have a bandwidth greater than the bandwidth required for the decoder/encoder 80 to operate in real time*." '459 patent at 7:39-42. Although PUMA's construction is similar, it is ambiguous as to what must "operate in real time." Defendants' construction provides that the decoder must operate in real time.[4]

C. "real time"

Defendants contend that the claims reciting "real time" are indefinite.

1. Law of Indefiniteness Requires "Reasonable Certainty"

In *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120 (2014), the United States Supreme Court set a new standard for assessing 35 U.S.C. § 112's definiteness requirement:[5]

> [W]e hold that a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Nautilus, 134 S. Ct. at 2123 (citation omitted). As the Supreme Court explained, the

[3] The Related Patents use reference number 70 for "bus" and "fast bus" interchangeably, i.e., "bus 70" and "fast bus 70." *See* 37 C.F.R. § 1.84(p)(4).

[4] All asserted claims that recite a "fast bus" also recite a decoder.

[5] Under section 112, "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention."

definiteness requirement performs an important public notice function:

> It cannot be sufficient that a court can ascribe some meaning to a patent's claims; the definiteness inquiry trains on the understanding of a skilled artisan at the time of the patent application, not that of a court viewing matters post hoc. To tolerate imprecision just short of that rendering a claim "insolubly ambiguous" would diminish the definiteness requirement's public-notice function and foster the innovation-discouraging "zone of uncertainty" . . . against which this Court has warned.

Id. at 2129 (citing *United Carbon Co. v. Binney & Smith Co*., 317 U.S. 228, 236 (1942)).

2. The Scope of Claims that Recite the Term "Real Time" Cannot be Determined with Reasonable Certainty

"Real time" appears in only five of the over 120 asserted claims.[6] Defendants do not dispute that, in some contexts, apart from those claims and the Related Patents, "real time" can have meaning.[7] However, in *this* context, a person of ordinary skill, having reviewed the Related Patents' specifications and prosecution histories, could not be reasonably certain as to the scope of claims that include "real time."

PUMA's analysis of "real time" rests on the term's prior construction in 2004. *See* PUMA Br. at 10-11. Defendants' argument, however, centers on statements made by the Applicants to the USPTO during prosecution of the '164 patent in 2013, *almost a decade after* that case. Dr. Stone's declaration, served prior to PUMA's brief,[8] explains why, because the Applicants made statements during the prosecution of the '164 patent concerning the defining

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[6] *See* claims 1 and 13 of the '789 patent, claim 1 of the '315 patent, and claims 1 and 6 of the '164 patent. The '164 patent and the '315 patent each incorporates by reference the '789 patent and share specifications with and claim priority to the '459 patent.

[7] PUMA's citation to use of "real time" in publications by Dr. Stone is irrelevant because the analysis of "real time" should be based on the intrinsic record. *See Nautilus*, 134 S. Ct. at 2123.

[8] The parties agreed that Defendants would provide an early declaration from Dr. Stone on indefiniteness, allowing PUMA to address Defendants' arguments in its opening brief. That declaration is mirrored in Ex. 2 at ¶¶ 1-28.

characteristic of "real time" that contradicted the patent specification, the term "real time" is indefinite to one of ordinary skill in the art. Rather than address that contradiction, PUMA's brief ignores it. PUMA Br. at 10-11. Instead PUMA argues definiteness based on the outdated, pre-*Nautilus* claim construction and extrinsic evidence, counter to both *Phillips* and *Liquid Dynamics*. In this case, it is the recent, contradictory, and confused *intrinsic record*—the primary source to which this Court must look—that renders "real time" indefinite under *Nautilus*.

a. According to the Specification, Bus Bandwidth Determines Whether "Real Time" Operation is Possible.

The asserted claims use "real time" to qualify how a bus transfers data between a decoder and a memory.[9] Every embodiment described in the Related Patents includes a "fast bus" for data transfers between a decoder and a memory to permit "real time" operation. *See* '789 patent at 6:58-60, 8:56-59, 9:19-22, 11:33-37; '459 patent at 5:14-20, 8:6-10, 9:60-64, 10:19-20. The '459 patent's specification defines a fast bus as "any bus having a bandwidth sufficient to allow the system [including the decoder] to operate in real time," '459 patent at 5:14-19, 6:63-67, and further provides that, to determine whether a bus's bandwidth is sufficient for such operation:

> The minimum bandwidth required for the decoder/encoder 80 can be calculated based on the characteristics and desired operation of the decoder, including the standard with which the bitstream is encoded to comply, whether the decoder/encoder 80 is to operate in real time, to what extent frames are dropped, and which images are stored. Additionally, the latency of the bus 70 that couples the decoder/encoder 80 to the memory 50 should be considered."

Id. at 7:42-50. The specification provides examples of fast buses that purportedly permit "real

[9] *See* '789 patent at cl. 1 ("the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time"); '315 patent at cl. 1 ("the bus having sufficient bandwidth to transfer data in real time between the shared memory and the decoder"); '164 patent at cl. 1 ("the memory bus configured to pass second data in real time between the shared main memory and the decoder/encoder").

time" data transfers between a decoder and a memory under at least *some* bandwidth calculations, including the industry standard PCI bus. '459 patent at 5:14-16.[10]

In short, according to the specification, whether a bus permits data transfers between a decoder and a memory in "real time" is determined from a bus's *bandwidth* as calculated from decoder and bus characteristics. Even PUMA's expert, Dr. Mangione-Smith, admits that "[t]he patents-in-suit expressed a concern that *bandwidth was the key bus performance factor* that needed concern" and "do not appear to be concerned" with latency. PUMA Br. Ex. J at ¶ 29. Thus, in light of the Related Patents' specifications' alone, a person of ordinary skill in the art would understand (1) a bus's bandwidth determines whether a bus satisfies a "real time" requirement and (2) a PCI bus is one example of a bus with sufficient bandwidth to satisfy a "real time" requirement. The prosecution history directly contradicts those understandings.

b. According to the Prosecution History, Bus Latency Determines Whether "Real Time" Operation is Possible

During prosecution of the '164 patent, Applicants' argued (1) a bus's latency, irrespective of bandwidth, determines whether a bus satisfies a "real time" requirement and, as a result, (2) a PCI bus does not satisfy a "real time" requirement. In particular, Applicants overcame a rejection based upon U.S. Patent No. 5,812,800 ("Gulick") by stating that a PCI bus was not "real time" because of *latency*:

> . . . *Gulick's* PCI devices must communicate with the main memory using **PCI bus 120, which is not a real time bus**. *Gulick at 5:29-38.* **Instead, the PCI devices 142, 144, 146 must obtain bus mastership, which consumes PCI cycles**. *Id.* The PCI devices in *Gulick's* FIG. 1 may communicate data between each other in real-time using the multimedia bus 130, but **this is different from claim 1, which calls out a memory bus configured to pass data in real time**

[10] One of the '459 patent's unasserted children outright claims a bus operating according to the PCI bus protocol as satisfying "real time" data transfer capability. Ex. 12 at cl. 1, 7.

between a shared main memory and a decoder/encoder.

Ex. 13 at PUMA0002591 (bold emphasis added). The reference to consumption of PCI cycles to obtain bus mastership is a reference to bus latency, a separate concept from bus bandwidth, Ex. 2, Stone Dec. ¶ 26. PCI, as an industry standard (Ex. 17), offers the same potential bandwidth regardless of whether it is recited in Gulick or the Related Patents. *See* Ex. 2 at ¶ 25. Rather than amend the claims, Applicants distinguished Gulick's PCI bus from the Related Patents' PCI bus based on latency regardless of bandwidth and contrary to the specification. Applicants' reliance on latency alone to evaluate "real time" created a new, undefined, and dispositive "latency" requirement within the meaning of the term "real time." PUMA must live with the consequences of the statement that allowed them to obtain the '164 patent claims.

3. Because the Prosecution History Contradicts the Specification, How "Real Time" Operation is Determined is Indefinite

Now, a person of ordinary skill in the art can only guess at the scope of a claim reciting "real time" and cannot determine it with reasonable certainty. *See Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) (finding an applicant's statement to the USPTO in a later application is relevant to the scope of the claimed invention in an earlier issued patent); *In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303, 1325 (Fed. Cir. 2011) ("we ordinarily interpret claims consistently across patents having the same specification"). Is "real time" strictly determined by bandwidth? By latency? By both, somehow? And, if by latency, how much latency is allowable? Such uncertainty violates the definiteness requirement's public notice requirement and falls squarely within the "zone of uncertainty." *Nautilus*, 134 S. Ct. at 2129. Dr. Stone's declaration provides three specific examples of how Applicants' statements prevent one of ordinary skill from understanding the scope of "real time" with reasonable certainty. In particular, it is uncertain whether those claims cover (1) a PCI bus (Ex. 2, Stone

Dec. ¶¶ 21-22); (2) other buses that meet a bandwidth requirement, including those exceeding the 400 Mbyte/s threshold (*Id.* at ¶¶ 23-25); and/or (3) other buses having bus latency that somehow violate this new and undefined latency requirement in "real time." (*Id.* at ¶¶ 26-27). For at least these reasons, "real time" as used in the Related Patents is indefinite under *Nautilus*.

4. PUMA's Expert's Analysis is Fatally Flawed

Significant flaws in Dr. Mangione-Smith's declaration reflect the difficulty of reconciling the intrinsic record. The Federal Circuit reiterated that "although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments." *Phillips*, 415 F.3d at 1323. Dr. Mangione-Smith runs afoul of *Phillips* when he limits his analysis of "real time" to a "very specific context with very specific bandwidth requirements" based on an aspect of an embodiment that Dr. Stone identified as falling within the "zone of uncertainty." *Id.* at ¶ 24. With that "very specific context," Dr. Mangione-Smith asserts "[c]learly, Gulick is concerned about executing a broader range of applications than the patents-in-suit" and is thus "about a different context." *Id.* at ¶ 25. Nothing in the claims or specification supports this "context" distinction. Dr. Mangione-Smith then applies Gulick's "real time" performance gauge—latency, not bandwidth—to re-distinguish Gulick from the then-pending claims of the application for the '164 patent. *Id.* at ¶¶ 29-30. But his reasoning is circular. It is the Related Patents' "real time" performance gauge—bandwidth—that should have controlled whether Gulick's disclosure of a PCI bus is "real time." Given that both Gulick's PCI bus and the "real time" PCI bus in the '164 patent conform to an industry standard, Gulick's PCI bus must fall within the scope of the "real time" claims. Contrary to Dr. Mangione-Smith's assertion that the patentees' contradictory statement is simply parroting Gulick, *id.* at ¶ 30, the patentees *affirmatively distinguish* Gulick's PCI bus from the claimed "real time" bus *based on latency*. Otherwise, if the Applicants were applying their bandwidth

gauge, their statement to the USPTO regarding PCI is flatly false.

5. Defendants' Proposed Alternative Construction

Should the Court determine that "real time" is definite, then the patentees must be held to their new latency requirement, and it must be factored into any construction for "real time." The only guidance on how latency impacts "real time" comes from the statement in the '164 patent prosecution history indicating the consumption of bus cycles while obtaining bus mastership excepts a bus from being "real time." Ex. 13 at PUMA0002591. Thus, Defendants' propose modifying PUMA's construction to account for those statements as follows: "fast enough to keep up with an input data stream, *wherein obtaining bus mastership does not consume bus cycles*."

D. "coupled," "coupleable," and "coupling"

1. The "Couple" Terms Should Be Limited to Attachments Involving No More Than One Bus

The dispute over "couple" does not involve, as PUMA contends, whether the word "couple" in general may refer to both direct and indirect connections. Rather, the real dispute is whether or not a "coupling" as used in the Related Patents includes more than one bus. The Applicants' consistent usage in the specification, claims, and prosecution history unequivocally indicates to one of ordinary skill that the "coupled" terms mean "attached, resulting in an arrangement that includes no more than one bus," as Defendants propose.

PUMA's reference to the construction of "couple" in other cases involving completely different patents than those at issue ignores the contextual use of "couple" in the Related Patents and also ignores the Federal Circuit precedent that the specification is the "single best guide to the meaning of the claim." *Phillips*, 415 F.3d at 1315.

A claim construction cannot be "divorced from the context of the written description and prosecution history." *Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1145 (Fed. Cir. 2005)

(consistent use of the term "board" to refer to wood cut from a log prohibits a finding that "board" could be construed to include synthetic materials); *see also id.* (citing *AquaTex Indus., Inc. v. Techniche Solutions*, 419 F.3d 1374, 1380 (Fed. Cir. 2005) ("Here, the context of the specification 'makes clear that the patentee did not intend the term [fiberfill] to encompass' natural materials.") (citation omitted)). "When a patentee uses a term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term 'by implication.'" *Bell Atlantic Network Serv's v. Covad Comm'ns Grp., Inc.*, 262 F.3d 1258, 1268 (Fed. Cir. 2001) (citation omitted). "Thus, the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive . . ." *Vitronics*, 90 F.3d at 1582.

PUMA seeks to stretch the reach of "coupled" to a scope never contemplated by the inventors. *See Ariad Pharm., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (inventor must have "possession of the claimed subject matter as of the filing date."). A claim term should not be read beyond the disclosed embodiments where such a reading is contrary to "the written description['s] . . . guidance as to the meaning of the claims." *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1344 (Fed. Cir. 2001) (where catheters in the art were either coaxial or side-by-side, and specification discussed only coaxial catheter, this "lead[s] to the inescapable conclusion" that only coaxial catheter is claimed); *see also Kinetic Concepts, Inc. v. Blue Sky Med. Grp., Inc.*, 554 F.3d 1010, 1018-1019 (Fed. Cir. 2009); *Wang Labs., Inc. v. Am. Online, Inc.*, 197 F.3d 1377, 1381, 1383 (Fed. Cir. 1999).

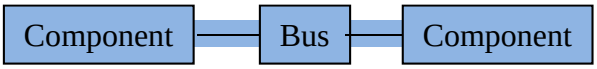
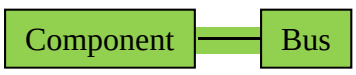
Here, the intrinsic evidence confirms that "couple" as used in the claims, refers only to those attachments that involve no more than one bus. The specification "consistently, and without exception" describes embodiments having characteristics that are critical to the invention. *Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1379 (Fed. Cir.

2006). In such situations, patentees may not extend their monopoly to matter lacking those characteristics. *Id.* (vacating construction broader than "overall context of . . . specification").

2. The Specification Describes "Couple" as an Attachment Involving No More Than One Bus

Here, Applicants used the "couple" terms repeatedly—236 times in the '789 patent and its file history, 47 times in the '459 patent and its file history, and similar numbers in each of the '459 patent's descendants—and consistently. In *every* instance, "couple" indicates only a particular arrangement for attaching components which includes *no more than one bus*. Whether direct or indirect, the "coupling" arrangement includes no more than one bus.

In the Related Patents, "couple" describes attachments in two general cases, either case 1: between two components, i.e., one component "coupled" to another component; or case 2: between a component and a bus, i.e. one component "coupled" to a bus. In the first case, where two components are "coupled," they are attached either case 1(a): directly to each other with no bus between; or case 1(b): with a single bus between the two components. In case 2, where one component is "coupled" to a bus, the attachment is direct, without using another bus in between the component and the bus. Two components, or one component and a bus, are *never* described as being "coupled" where more than a single bus is used to attach them. The table below illustrates these three scenarios. The coupling always results in no more than one bus.

Component-to-Component "Coupling"	**Component-to-Bus "Coupling"**
Case 1(a)  Case 1(b) 	Case 2 

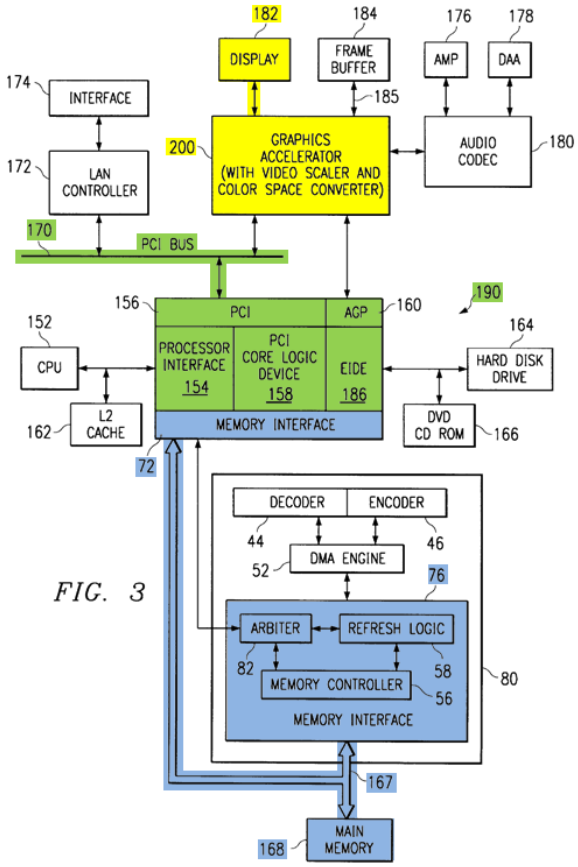


FIG. 3

'459 patent, Figure 3 (highlighting added, as discussed in following paragraphs).

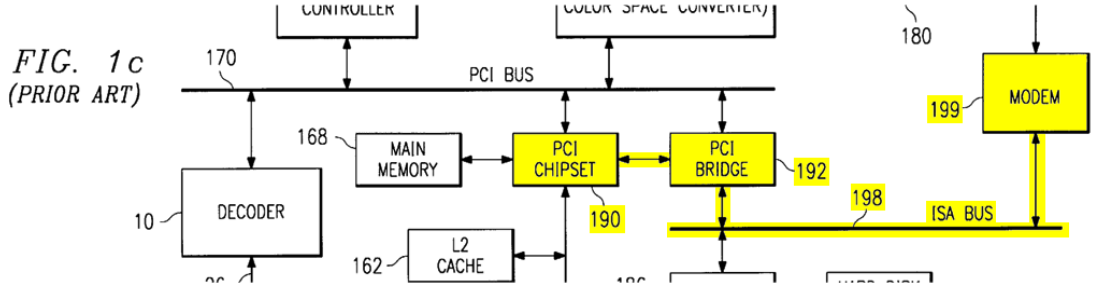
To illustrate case 1(a) as highlighted yellow, the '459 patent states that: "[t]he graphics accelerator 200 is *coupled* to a display 182 . . ." '459 patent at 10:5-7 (emphasis added). This coupling arrangement includes direct attachment with no bus. *See also, e.g.*, 7:1-2, 10-11, 16-17.

To illustrate case 1(b), highlighted in blue, the '459 patent states that: "[t]he main memory 168 is *coupled* to the memory interfaces 72 and 76 through a memory bus 167." '459 patent at 9:60-61 (emphasis added). This coupling arrangement includes one bus—a memory bus. *See also, e.g.*, 4:59-60; 8:6-8.

To illustrate case 2, highlighted in green, the '459 patent states that: "[t]he core logic chipset 190 is *coupled* to . . . a bus such as a PCI bus 170 . . ." '459 patent at 9:53-57 (emphasis added). This coupling includes one bus—PCI bus. *See also, e.g.*, 9:46-49, 10:3-5.

Thus, *every* usage of "couple" in the specification and claims consistently results in an

arrangement that includes *no more than one bus*. Indeed, seeking (but failing) to find a counterexample, PUMA in its brief points to the coupling between modem 199 and core logic (PCI chipset) 190 in an attempt to show a *single* instance where two components are "coupled" in an arrangement involving *more* than one bus. *See* PUMA Br. at 18. PUMA argues that the arrangement includes "two buses." But plainly, it does not. The modem 199 is coupled to the PCI chipset 190 via ISA bus 198 and PCI bridge 192, an attachment resulting in *no more than one bus*. As shown below, the PCI bridge 192 and PCI chipset 190 are directly connected. Nothing in the specification suggests that the PCI bus 170 is involved in coupling between the modem and PCI chipset. Yet again this is a coupling between two components that results in an arrangement including *no more than one bus*, i.e., in this example ISA bus 198.



'789 patent, Figure 1c (excerpt highlighting coupling between modem 199 and PCI chipset 190 involving no more than one bus, namely ISA bus 198).

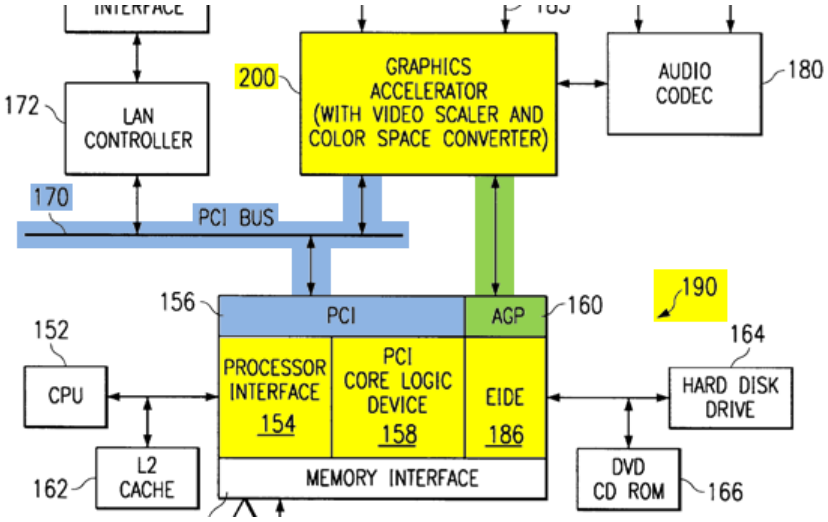
3. The Claims Describe "Couple" as an Attachment Involving No More Than One Bus

The claims also indicate that Applicants indicated "couple" to involve just one bus, by using "couple" to refer to a singular-bus arrangement. *See, e.g.*, '789 patent, claim 1: "*a shared bus coupled to* the memory, the first device, and the decoder . . .," claim 13: "The electronic system of claim 1, wherein *the bus* has a bandwidth . . ."; '368 patent, claim 1: "*a bus coupled to* the memory"; '164 patent, claim 1: "core logic *coupled by a first bus . . . a memory bus coupled to* the first memory interface . . .," claim 6: "The computing device according to claim 1 wherein

the memory bus is capable of . . . .” Other claims are similar. The claims are all written to limit the coupling to “a bus,” “the bus” or “the memory bus,” i.e., a single bus.

Further, the claims make clear that a single bus was contemplated for coupling components. In particular, ’164 patent claim 1 includes a “first bus” that couples a CPU, cache memory, and core logic together, and separately, a “memory bus” that couples a “first memory interface” that is part of the core logic to a “second memory interface.” But in each case, components are “coupled” in an arrangement that includes no more than one bus.

Claim 13 of ’164 patent requires “a graphics accelerator *coupled* to the core logic via an Accelerated Graphics Port (AGP) bus[11] *and* a Peripheral Component Interconnect (PCI) bus . . .” But again, Applicants used “coupled” to describe an attachment involving one bus—here a PCI coupling and an AGP coupling each involve one bus. Figure 3 shows graphics accelerator 200 coupled to core logic 190 through PCI (blue) and, separately, through AGP (green).

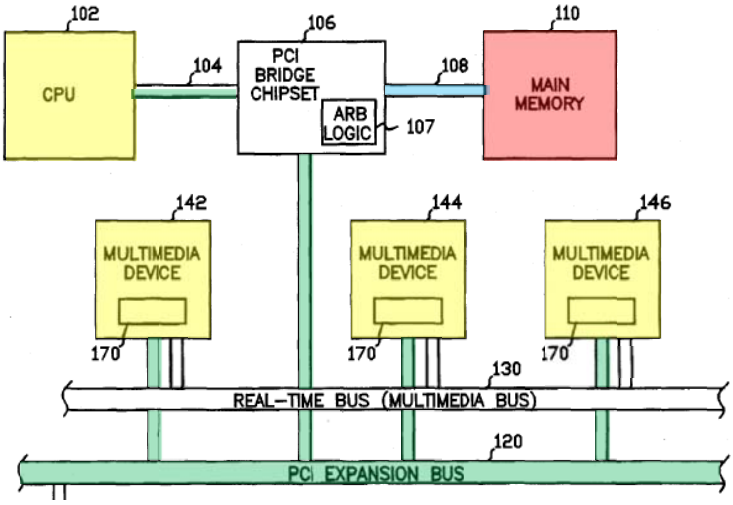


’459 patent, Figure 3 (excerpt, highlighting added).

[11] Defendants note that, per the Applicants’ prosecution characterization, the AGP interconnection is not a bus since it connects only two components, as captured by Defendants’ proposed construction. *See supra* § IV.A.3.

4. The Prosecution History Describes "Couple" as an Attachment Involving No More than One Bus

In addressing the Examiner's rejection of pending claims in the '459 patent as anticipated by Lambrecht (*see* Ex. 4 at PUMA0000686-87), Applicants stated, "[t]he present claims are directed toward systems and methods for providing *direct access* for a first device and decoder to a first memory. . . . Unlike the claimed invention, [Lambrecht] uses a PCI bridge chipset for access between other first devices or decoders and a main memory." Ex. 5 at PUMA0000762-64 (emphasis added). The pending claims required, in relevant part "a decoder coupled to the first memory to provide direct access to the first memory . . ." *Id.* at PUMA0000756. Thus, Applicants argued that the PCI bridge chipset of Lambrecht defeated the "coupling" between the decoder and the memory. However, as illustrated below, Lambrecht's CPU 102 (a "first device"/decoder in yellow) is attached to main memory 110 (red) via *two buses*—i.e., CPU local bus 104 (green) *and* memory bus 108 (blue). The CPU does not have "direct access" to the main memory, because it is attached through *two buses* and thus *it is not "coupled."* Likewise, the Multimedia Device 142/144/146 (an alternate "first device"/decoder in yellow) is also attached to the main memory 110 via *two buses*—i.e., PCI expansion bus 120 (green) and memory bus 108 (blue). *See* Lambrecht, Ex. 3 at 7:29-44.



During the ’368 patent prosecution, Applicants characterized “the present invention” as having “both the decoder 80 and the device 42 . . . *directly* coupled to the fast bus 70, which in turn is coupled to the memory 50.” Ex. 14 at PUMA0001256. Thus in “the present invention” devices are “coupled” only via one bus. Applicants rejected the notion of *indirect* coupling as PUMA now proposes. Characterizations of “the present invention” are generally considered binding because they describe not merely *an* embodiment, but what the Applicant considers to be their “invention.” *Honeywell Int’l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006). In a USPTO Board appeal brief, Applicants reiterated the same notion: “Since the same bus is concurrently coupled to both of the devices, both of them have the ability to place data on and retrieve data from the bus 70, each of them having *direct access* to the fast bus 70.” Ex. 15 at PUMA0001279. Every description of “couple” involves *no more than one bus*.

Notably, Applicants distinguished references as not providing “direct access” between the decoder and memory during prosecution of pending claims containing the phrase “communicatively linked . . . without requiring a second bus” (e.g., claims of the ’459 and ’194 patents; Ex. 5 at PUMA000763-64) *and* claims containing “coupled” (e.g., the ’368 patents and descendants; Ex. 15 at PUMA0001282). Because they made the same argument for two separate terms used to link the decoder and memory, Applicants clearly intended “coupled” to be coextensive with “communicatively linked . . . *without requiring a second bus*,” i.e., attached in an attachment resulting in no more than one bus.

5. PUMA’s Arguments Lack Merit

In contrast, PUMA argues first that no construction is necessary for “couplable,” “coupled,” and “coupling.” A construction is necessary for this term at least because the parties disagree as to the meaning of the term. *O2 Micro Int’l v. Beyond Innovation Tech.*, 521 F.3d 1351, 1362-63 (Fed. Cir. 2008) (“When the parties present a fundamental dispute regarding the

scope of a claim term, it is the court's duty to resolve it."). If a construction is necessary, PUMA proposes that "coupled" be construed as "directly or indirectly connected." This construction is incorrect because, not only it does fail to inform the dispute, but PUMA may also be setting up an attempt to argue later that a coupling connection could encompass *more than one bus*, contrary to the entire intrinsic record.

Ignoring the specification, which is replete with instances of "coupled," PUMA resorts to other cases construing the term in a different context. *See* PUMA Br. at 15. However, this ignores the Federal Circuit precedent that the specification is the "single best guide to the meaning of the claim." *Phillips*, 415 F.3d at 1315. Here the specification's repeated and consistent usage of "coupled" indicates a bounded arrangement between two components that includes *no more than one bus*.

Moreover, PUMA's proposed "direct or indirect" construction finds no support in the specification, claims, or prosecution history. PUMA cites no instance, and indeed there are none, where the intrinsic evidence suggests an unbounded number of layered connections or multiple buses. Such a boundless "coupling" provides no guidance to the Court or jury as to just how "indirect" an "indirect connection" can be. Instead, PUMA argues that "attached" and "arrangement" are unclear. PUMA Br. at 17-18. These are red herrings. In the claims, the word "couple" is used in the context of connecting or attaching components. Defendants' construction is consistent with the context in which it appears and adds meaning by clarifying how the components are attached by describing the resultant arrangement consistent with the intrinsic record. Defendants' construction clarifies that the coupling must include *no more than one bus* because that is what the specification and the prosecution history mandates. The "boundaries" which perplex PUMA are clearly the devices being coupled.

E. "directly supplied and "directly supplies"

Defendants propose construing "directly supplied" and "directly supplies" as "provided via a single bus with no intervening components," and "provides via a single bus with no intervening components." Again, in every case, the usage of "directly supplied/supplies" is similar. Images are "directly supplied" to a display adapter from a decoder. Figure 4 of the '789 patent illustrates how bidirectional images "B" are provided from the Decoder/Encoder 80 to the Video Controller 120 via PCI bus 170. These components are highlighted below.

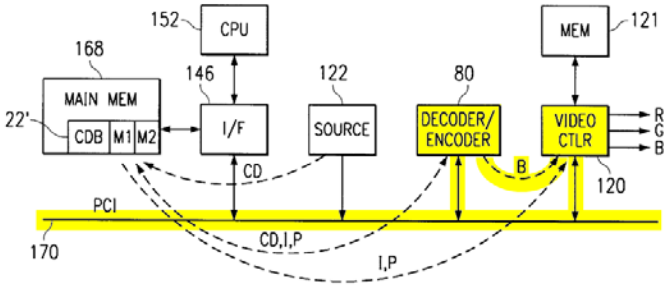


FIG. 4

The dashed curved line between the decoder 80 and video controller 120 indicates that decoded bidirectional images are supplied to the video controller for display. As the specification states, "[i]n the case where the compressed data correspond to bidirectional 50 images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data." '194 patent at 10:48-51. The decoder 80 "directly supplies" images ("B") to the video controller 120 because the images are supplied via a single bus, namely PCI bus 170, with no other intervening components. Thus, Defendants' proposed construction is consistent with the usage in the specification and claims.

In contrast, PUMA argues first that no construction is necessary for "directly supplied/supplies." A construction is necessary for this term, at least because the parties dispute its meaning. In the alternative, PUMA proposes that "directly supplied/supplies" should be construed as "supplied without being used in the decoding of subsequent predicted or

bidirectional images." PUMA's construction, however, ignores the plain language of the claim read in light of the specification. For example, claim 15 of the '194 patent states: "the images *directly supplied to the display adapter* being bidirectional images obtained from two preceding intra and predicted images" (emphasis added). The image being "directly supplied" is indicated by the 'B' in Figure 4 below, between the "Decoder/Encoder" 80 and the Video Controller 120.

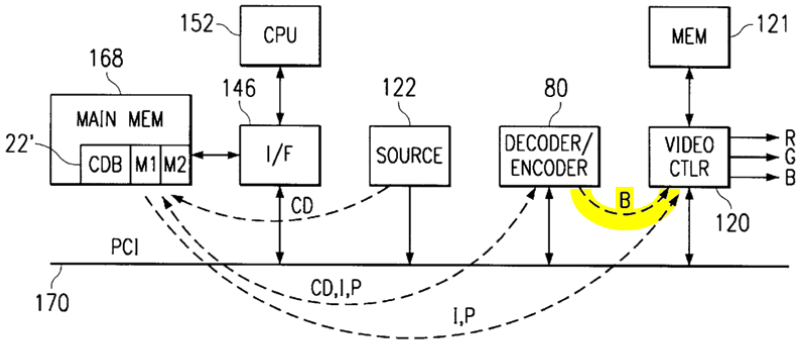


FIG. 4

The bidirectional image 'B' is directly supplied, i.e., not indirectly supplied, not simply because it is "not used in coding subsequent or bidirectional images," but because it is supplied via a single bus with no intervening components. This is in contrast to the prior art in Figure 1c where bidirectional images B are stored in the decoder's local memory 22 and must pass through decoder 10 (an intervening component), across bus 170, and then to video controller 120.

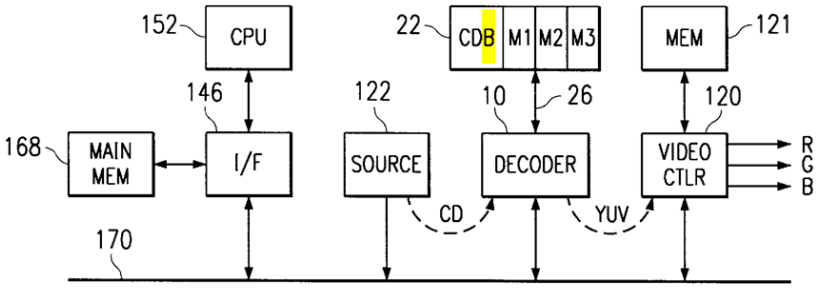


FIG. 1c
(PRIOR ART)

Accordingly, "directly supplied/supplies" should be construed as "provided/provides via a single bus with no intervening components."

F. "display device" and "display adapter"

Defendants address "display device" and "display adapter" together to illustrate the specific dispute. The parties agree that a "display device" includes a "screen." The dispute is whether "display device" is "a device for displaying images or video," as Defendants propose, or whether it *additionally* encompasses "*associated* display circuitry," as PUMA proposes.

"[A]ssociated display circuitry" is a term PUMA appears to have pulled out of thin air and for which there is no support. Apart from the claims, the only textual support for "display device" in the specifications is as follows: "The display adapter then supplies these to a *display device* such as a screen." *See* '459 patent at 10:40-41. This, however, confirms a "screen" is an example of a "display device," and a "display device" is *distinct* from a "display adapter." This second point is further supported by Figures 1c and 4 of the '459 patent, which show "Video Ctlr" (display adapter 120), but not a display device.

PUMA's "associated display circuitry" allows ambiguously for a "display device" to include a "display adapter," which would invariably be "*associated*" with the display—which cannot be correct, since the specification makes clear that the "display adapter" supplies images "to" the display device, i.e., they are separate devices.

Regarding "display adapter," the parties agree that such an adapter processes images. PUMA, however, criticizes Defendants' proposal for use of the term "adapter"; but PUMA's proposal again attempts to define "adapter" as a "circuit, " albeit without support. PUMA points to statements in the specification that "display adapters" are "interfaces" that "make it possible to directly process the 'YUV' (luminance and chrominance) image data normally supplied by a decoder," concluding that "a 'display adapter' is a *circuit* for processing images." There is simply no support for PUMA's proposal to include a "circuit" in "display adapter."

G. "control circuit"

This dispute boils down to whether the "control circuit": (1) is an *electronic device* that (2) is *separate from* the CPU/processor and (3) *interacts with* the operating system. In describing "the present invention," the patentee confirmed all three characteristics:

> Broadly stated, *the present invention embodies a control circuit* for use in a computer system. The computer system is controlled by an operating system and has a main memory. *An electronic device is coupled to the processor* and the main memory *and is configured to request* continuous use of several portions of the main memory *from the operating system*.

'464 patent at 3:37-43 (emphasis added). This passage sums up the uniform disclosure of the '464 patent specification. The drawings tell the same story. Element 114 in Figure 1 is "an MPEG 2 decoder under the present invention," an expanded view of which is shown in Figure 2:

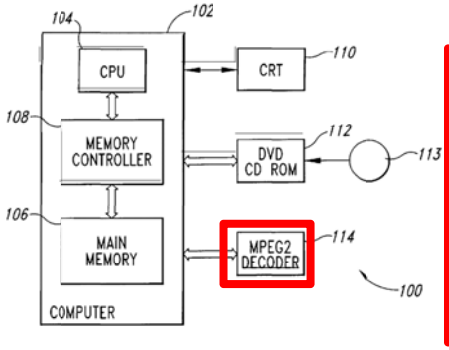


Fig. 1

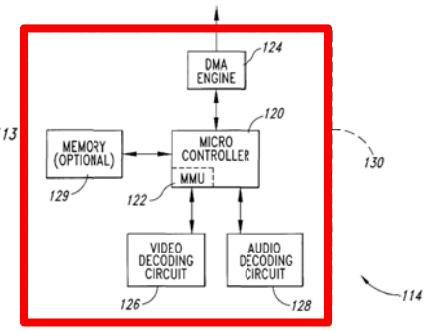


Fig. 2

The '464 patent uniformly discloses microcontroller 120 inside MPEG decoder 114 as the entity that requests memory from the operating system and translates between noncontiguous and contiguous addresses—the tasks of the claimed "control circuit." *See, e.g.*, '464 patent at 6:63-7:50. Figures 1 and 2 confirm that the entirety of MPEG decoder 114, including microcontroller 120, is not part of CPU 104, the operating system, or even computer 102—instead, the MPEG decoder is a separate device coupled to computer 102 just like CRT (display) 110 and DVD/CD ROM player 112.

The patentee repeatedly and consistently characterized this divided architecture as "the

present invention." *See, e.g.*, '464 patent at 1:19-20 ("The present invention relates to the field of *electronic systems* requiring blocks of memory"); 6:60-62 ("the present invention *shares* the main memory 108 *with the computer 102*"); 9:14-21 ("The present invention *interacts with the Windows 95 operating system* 152 to *act like* a software application" but "*actually employs hardware*" that "*is not a CPU*, or other processor, or Intel-based microprocessor") (all emphasis added). These repeated and consistent representations belie PUMA's claim that no construction is necessary. *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention.").

Applicants continued their consistent message during prosecution, specifically arguing the separateness of the "control circuit" to the Patent Office to gain allowance. In response to a rejection, Applicants amended independent claim 25 to include the "control circuit" and argued that "Herrell et al. does not teach the administration of a memory management method through a *separate control circuit* . . ." Ex. 16 at PUMA0000506-7 (emphasis added).[12]

PUMA's arguments range from flawed to irrelevant. First, PUMA argues that construing "circuit" as "device" is "unhelpful." PUMA Br. at 26. To the contrary, not only is "device" the very word the patent uses to describe the claimed "control circuit" (3:40-43), such a construction unquestionably grounds the "control circuit" in the realm of the physical, not merely a piece of software running on the operating system. Again, "[t]he present invention relates to the field of

[12] To demonstrate on an even more fundamental level why structural boundaries matter for this term, claim 25 is a method claim, and the patentee amended the claims both to add the structural limitation of a "control circuit" and to require the "control circuit" to perform the steps of the method. Ex. 16 at PUMA0000506. Thus, for the amendment to meaningfully limit the claim, the "control circuit" must be something different than the other elements already present in the claim (e.g., the processor).

electronic systems requiring blocks of memory." '464 patent at 1:19-20 (emphasis added). Making that distinction clear will be very helpful to the jury.

Second, PUMA argues that the jury would be confused because the patent does not explain what it means for two things to be "separate." PUMA Br. at 26. PUMA's point is unclear. As shown above, the patentee used the word "separate" to distinguish prior art and thus limited the claims accordingly. The fact that the patent does not provide a special definition for "separate" simply reinforces the fact that the jury should be well-equipped to understand the word based on common parlance—just as the Examiner presumably did.

PUMA's appeal to not construe this term portends mischief at trial. PUMA alleges that the surrounding claim language adequately defines "control circuit," but the examples it provides appear on their face to reinforce Defendants' proposed construction (e.g., "the 'control circuit' is coupled . . . to the processor" and "configured to 'request . . . from the operating system.'"). In other words, there should not be a dispute. The fact that there is one suggests that PUMA wants the flexibility for its expert to tell the jury that hardware can be "coupled to" a processor while itself being part of that processor, and/or that software can "request" something from the operating system while itself being part of that operating system. The Court should resolve this dispute now rather than allowing PUMA to argue it to the jury. *O2 Micro*, 521 F.3d at 1362-63.

H. "algorithmically translate the noncontiguous addresses to the contiguous addresses"

PUMA presents two alleged disputes: (1) how many mathematical operations must be performed, and (2) on what they must be performed. Neither is a real dispute.

How many: The parties' agree that to "algorithmically translate" something involves at least one mathematical operation. There are multiple "somethings" being algorithmically translated in the disputed claim term—"addresses." Thus, simple English parallelism requires

plural "mathematical operations," i.e., at least one per address. Defendants' construction does not seek to require that multiple mathematical operations be performed on a given address.

On what: The claim language itself says that the noncontiguous addresses are what are being "algorithmically translated." Thus, of necessity, the mathematical operation(s) the parties agree are involved in algorithmic translation must be performed *on the noncontiguous addresses*. PUMA's own example from the patent performs addition *on the noncontiguous addresses* to map them to the block of contiguous addresses. PUMA Br. at 27. And indeed it must be so: any mathematical equation that "translates" a first address (a number) to a second address (a different number) will by definition contain the first address. PUMA's appeal to the well-worn language, "nothing in the claims, the specification or the prosecution history . . .," PUMA Br. at 28, does not obviate common sense.

V. CONCLUSION

Defendants respectfully request the Court adopt their proposed claim constructions and find "real time" indefinite.

Dated: April 21, 2015

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on April 21, 2015.

/s/ Smith R. Brittingham IV